Network Card Mk II
Interface Specification

Title:	Network Card Mk II Interface Specification
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Contents

1. Introduction

This document describes the outline specification for a network card for use with Acorn Computers. This interface provides a route for adding networking capabilities such as cheapernet. Intel type PC signals are provided via a connector to the mother board and space on the backpanel for the output connector.

2.Cost/performance

The very high performance requirements of file severs etc will require networking via the higher cost general expansion route. This interface does provide the ability to have software code loaded from an EPROM on the card. It also provides a 16 bit wide data bus. This interface is aimed at providing good performance networking at a low cost.

3. Description of signals

Convention used. An active low signal is indicated by a N. An input has a signal direction from the motherboard to the network card. The reverse is an output.

Name	Function	Signal Threshold
rst	Reset input	TTL level
Nior	I/O read input	TTL level
Niow	I/O write input	TTL level
bd[15:0]	Peripheral data bus bidirectional	TTL level
Interrupt	Interrupt output. Level triggered, programmable	TTL level
ready	Cycle Stretch or ready signal (low to extend cycle) output - open drain	TTL level
Ncsnet	Network chip select input	TTL level
la[9:2]	Latched addresses input	TTL level
Nromnet	ROM select strobe input	TTL level
Psp[8:1]	Product specific pins	TTL/Analogue

Product specific pin definitions and assignments are listed in Appendix B of this specification.

These signals are provided by a half size DIN 41612 - 48 way type R connector providing three rows of sixteen pins. It is recommended that it has a double wipe contact with gold flash as a minimum. The pin list given below is the connector pin numbering to be found on the mother board pcb. The mating pair to this is available in two types. **The connector with the required dimensions will have reversed pin numbering** i.e. pin 1 is labelled pin 16.

Pin	Row A	Row B	Row C
1	Bd3	Nromnet	Bd4
2	Bd2	0v	Bd5
3	Bd1	Bd6	Bd0
4	Bd7	0v	Psp1
5	Psp2	Bd8	Bd9
6	Bd10	0v	Bd11
7	Bd12	Bd13	Bd14
8	Bd15	0v	+5v
9	Psp3	Psp4	Psp5
10	+5v	0v	La3
11	La4	La6	La2
12	La7	0v	La5
13	La9	Rst	La8
14	Psp6	Psp7	Psp8
15	Ready	0v	Interrupt
16	Niow	Nior	Ncsnet

4. Power limitations

The following table gives the power available for the networking card. These figures are based on two factors, (1) the capabilities of the power supply and (2) the thermal capacity of the case.

	Inside machine	External
Network card	600mA	0 mA

Any proportion of the internal current may be dissipated externally to the machine.

5. Network Card ROM

The Network Card specification has provision for software driver code to be loaded from a ROM on the card. This ROM will be read by the 'network manager' software on 'power-on'.

The ROM will be 8 data bits wide and will be addressed using the following scheme or an arrangement providing the same functionality. A 12 bit counter is used to provide the lower 12 address lines to the ROM. The counter is reset to zero by the reset line or by writing to the ROM address space. The Card is now ready to have the ROM accessed. A read of the ROM address space will provide the data contained in the first location. The end of the read cycle is used to automatically move the counter along by one count. A further read of the same address will provide data in location two. In this way 4096 ROM locations can be accessed using the same address before the counter is zero again. The ROM page size is therefore 4096 bytes.

Direct address lines La2 to La9 are provided by the interface. Connection of these to the upper address lines of the ROM provides access to 256 pages giving a possible maximum ROM size of 8Megabyte.

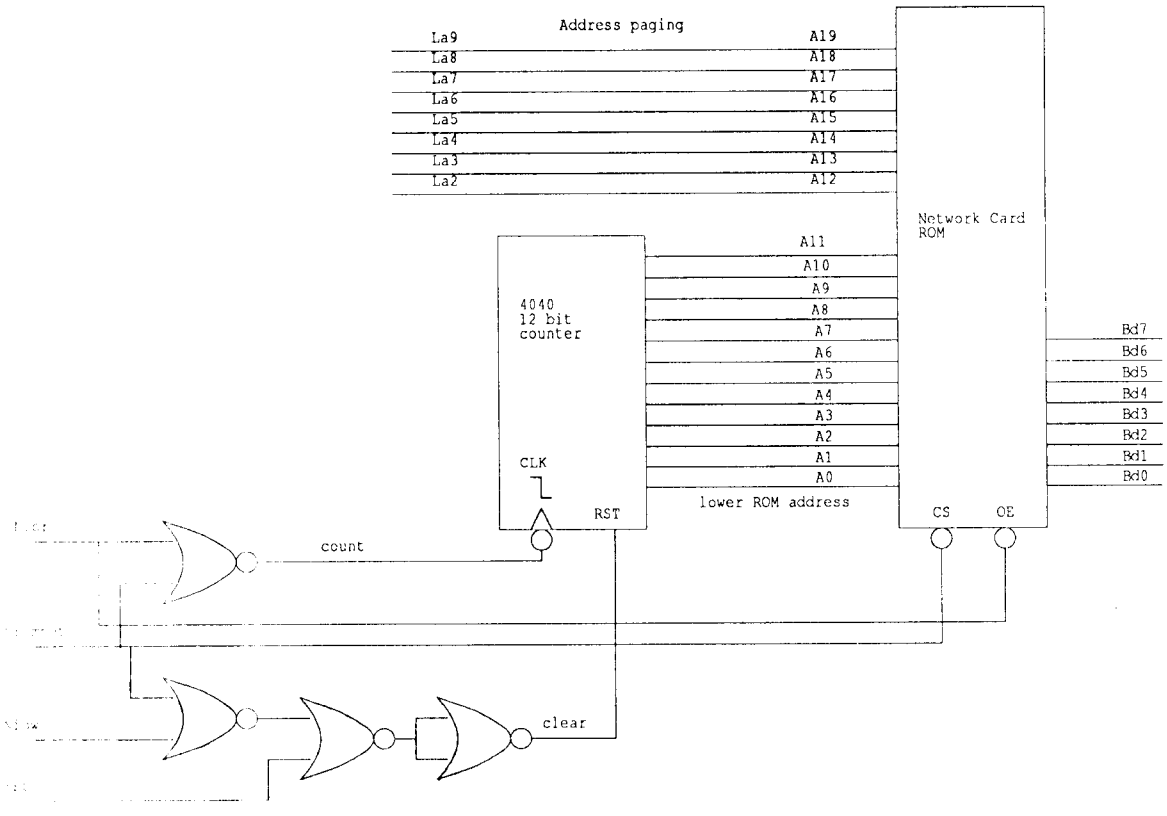
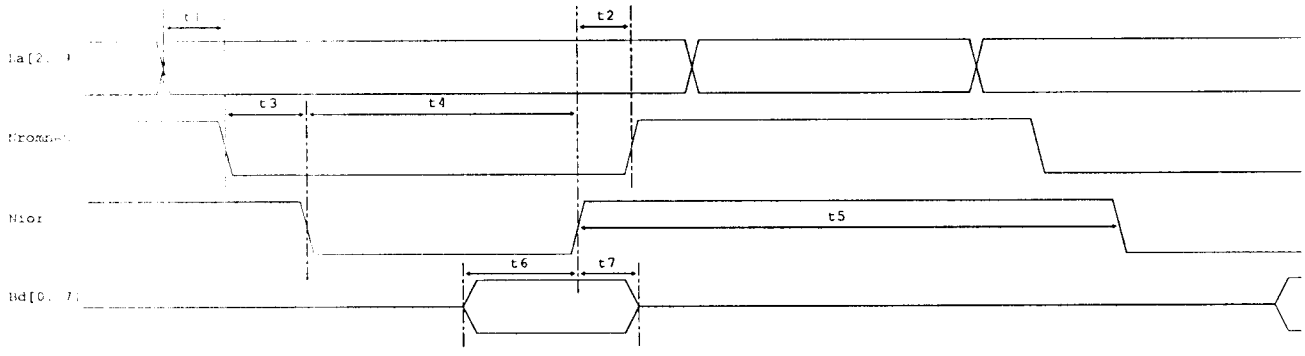


Figure 1. Recommended ROM addressing circuit.

Figure 2. ROM addressing timings.



Sym.	Description	Min.	Typ.	Max.	Units
t1	Address setup to Nromnet	10			nS
t2	Nior high to Nromnet high	10			nS
t3	Ncsnet low to Nior low	10			nS
t4	Nior strobe	180			nS
t5	Nior high to Nior low	250			nS
t6	ROM data setup to Nior high	20			nS
t7	ROM data hold from Nior high	5			nS

6. Memory Map

On the Risc PC product the address decode is as follows :

I/O Address (Hex)	Contents
0302 B000 to 0302 B3FF	Nromnet address space
0302 B800 to 0302 BBFF	Ncsnet address space

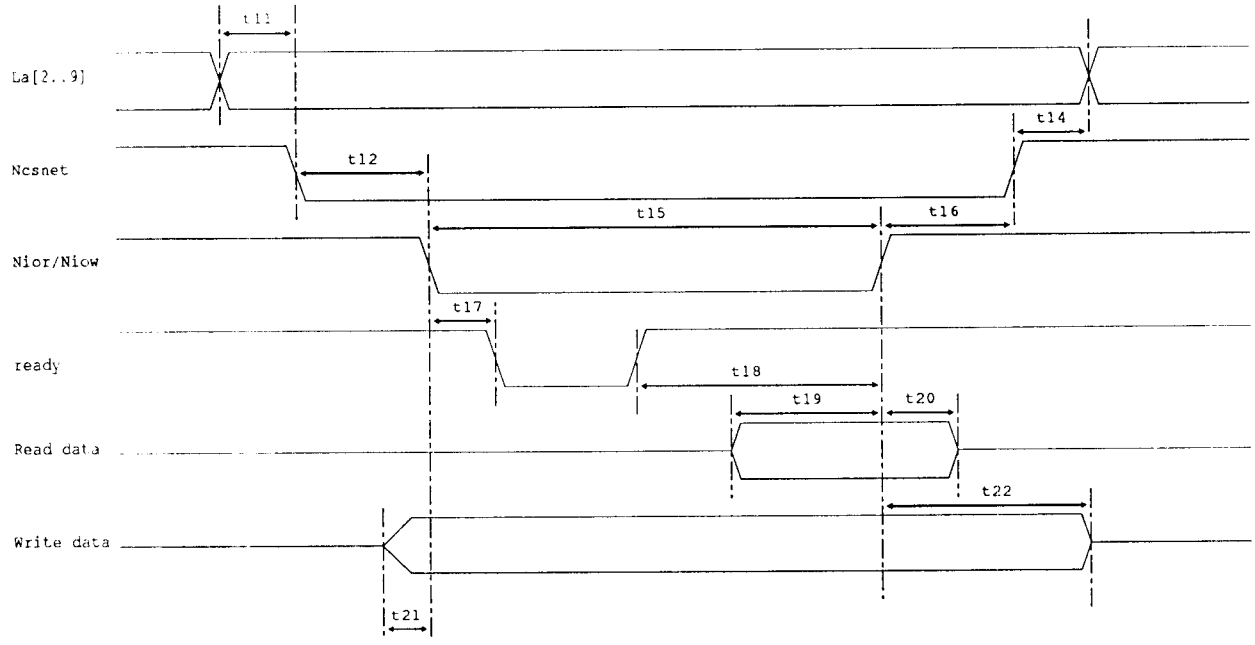
7. Firmware Support

Full details of extended address space ROM headers are given in the document **Expansion Interface Software** (Acorn reference number 0197,269/FS).

8. Signal Specification

The signals are similar to a cut-down PC-AT bus (i.e. Intel-style control signals, read strobe, write strobe, etc).

Figure 3. Signal timings.



Sym.	Description	Min.	Typ.	Max.	Units	notes
t11	Address setup to Ncsnet	10			nS	
t12	Ncsnet low to Nior or Niow low	10			nS	
t14	Address hold from Ncsnet high	20			nS	
t15	Nior and Niow strobe width			255	nS	(i)
t16	Nior or Niow high to Ncsnet high	10		95	nS	
t17	Nior or Niow low to ready low	30			nS	(ii)
t18	ready high to Nior or Niow high			125	nS	(ii)
t19	Read data setup to Nior high	20			nS	
t20	Read data hold from Nior high	5			nS	
t21	Write data setup to Niow low	0			nS	
t22	Write data hold to Niow high			25	nS	

notes.

(ii) The ready signal is used to stretch the present cycle if required. The maximum timings given are for non-stretched cycles.

(i) There are two important timings associated with the stretched cycle. If the ready signal is not asserted early enough in the cycle this signal will not be seen and therefore the cycle will continue to complete without being stretched. When the stretched cycle is ready to be completed there is a variable delay between deasserting the ready signal and this being synchronised to the main system for completing.

Interrupt timings.

Interrupts are programmable and therefore the time between an interrupt request and it being serviced is not possible to specify in this type of document. Seek direct technical support if this is likely to be a problem. An Interrupt signal must be removed (cleared) within 250 nS of the software instruction initiating this action.

Note DMA is only available on product variant A - see Appendix B.

Figure 4. DMA Timings 1

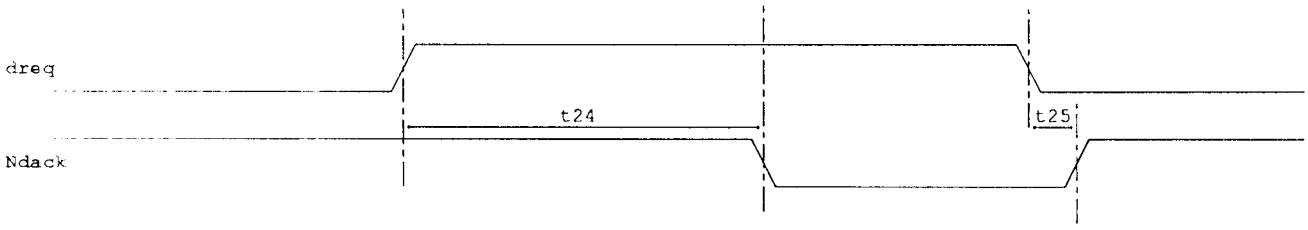
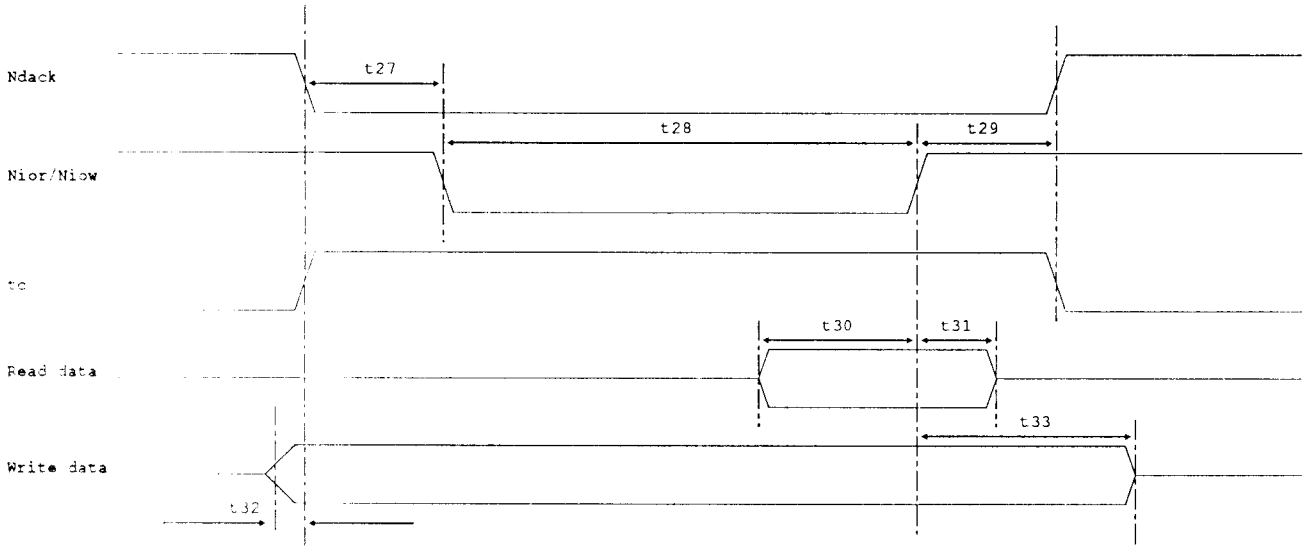


Figure 5. DMA Timings 2



Symb	Description	Min.	Typ.	Max.	Units
t24	dreq high to Ndack low			100	nS
t25	dreq low to Ndack high	10			nS
t27	Ndack low to Nior or Niow low	10			nS
t28	Nior and Niow strobe width			255	nS
t29	Nior or Niow high to Ndack high	10		95	nS
t30	Read data setup to Nior high	20			nS
t31	Read data hold from Nior high	5			nS
t32	Write data setup to Niow high	0			nS
t33	Write data hold to Niow high			25	nS

8.1 Signal tracking

It is recommended that all bus signals that are to be used on multiple inputs far from the connector are buffered. The buffer devices should be physically close to the signal connector.

Signals should not be presented with a capacitive load greater than 20pF, this is equivalent to the connector (5pF), 6cm of 0.2mm copper track (5pF), and 10pF input capacitance of the buffer device (eg 74HC245 for data lines). Unidirectional buffers will have lower input capacitance (typically 3.5pF). Tracks should always be kept as short as possible.

This gives worst case rise and fall times for all data bus signals of 12nS. Other signals will be equal or better.

9. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Condition
Digital signals						
Low-level input voltage	V_{IL}			0.8	V	V_{cc}=4.75v
High-level input voltage	V_{IH}	2.0			V	
Low-level output voltage	V_{OL}		0.15	0.26	V	I_{OL} = -4.0mA
High-level output voltage	V_{OH}	3.5			V	I_{OH}=Max V_{cc}=4.75
High-level output current	I_{OH}			-400	uA	V_O = 3.0v V_{cc}=4.75v

Analogue Signals

Source impedance 2K2 Ohms (min) to 200K Ohms (max)

Output Voltage range 0 to +5V DC

Frequency range DC to 50Hz

10. Space limitations

This interface has to fit in a limited space and therefore it is very important to make sure that the limitations as given below are adhered to. The following three diagrams give the required information. Diagram 1 shows a view looking down on the main pcb giving the location of the socket. Diagram 2 gives the maximum dimensions of a networking card and the location of the connector. Diagram 3 gives the dimensions of the maximum usable space above and below the networking card.

Diagram 1

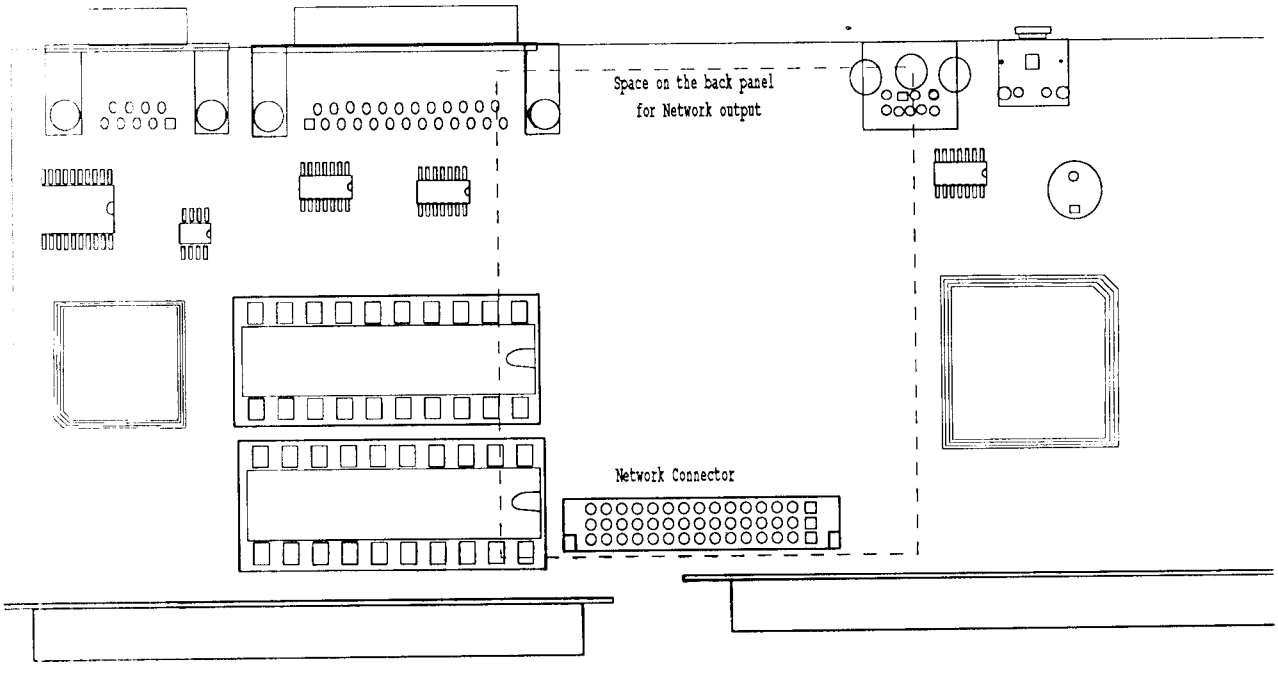


Diagram 2

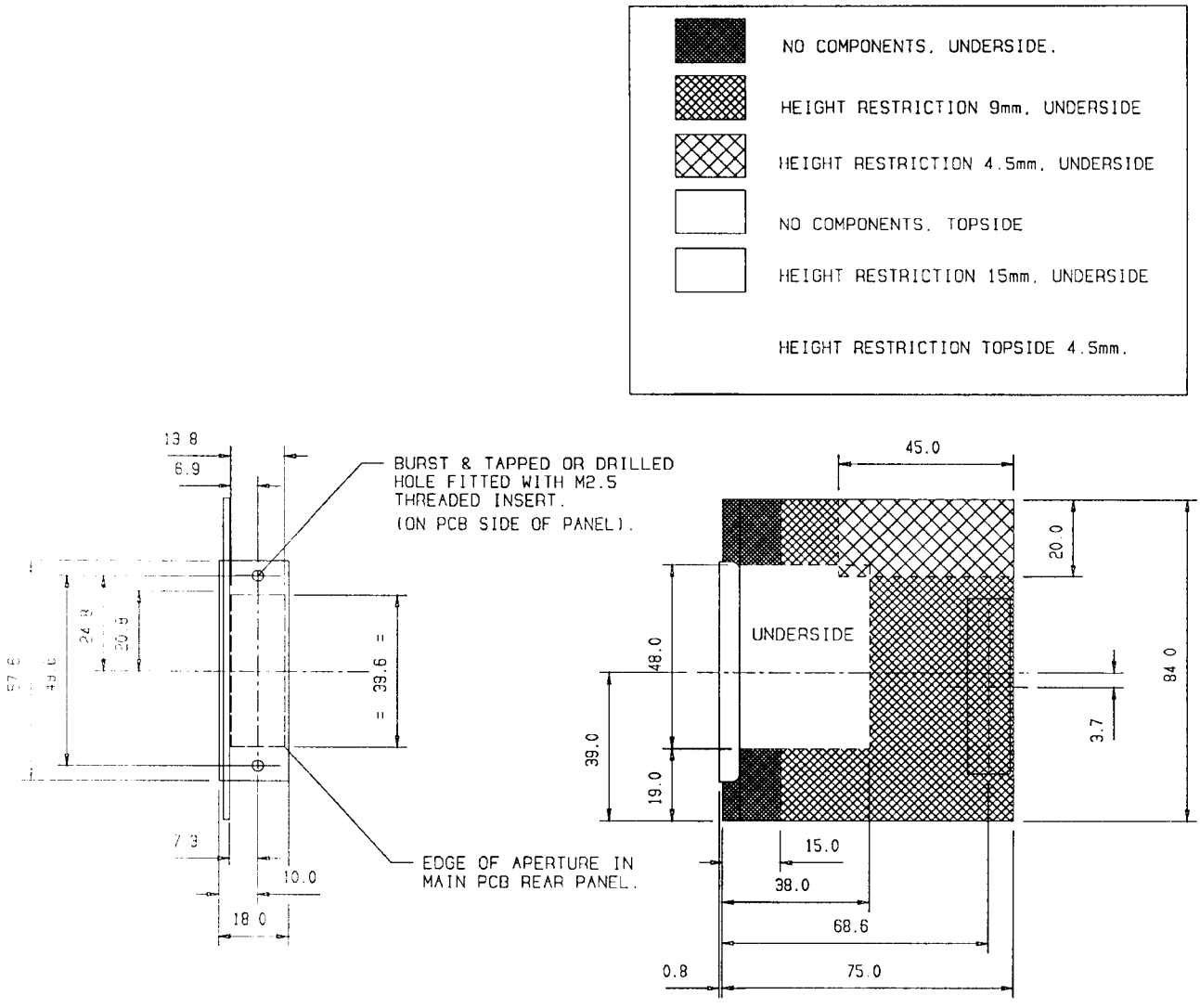
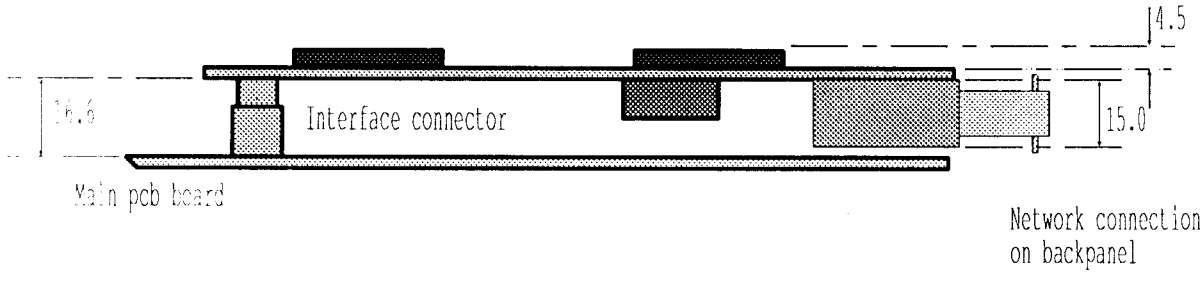


Diagram 3



All dimensions in millimetres

11. Airflow

As can be seen from the mechanical details local heating problems may be encountered due to trapped air between the main pcb and the network card. It is recommended that careful consideration is given to the layout of the network card to allow airflow between these two boards.

12. Isolation

Some network specifications require there to be electrical isolation between the network and the computer. This will be possible as the card will have its own backpanel space. The isolation area should be keep as close to the backpanel as possible. This is the area where the main pcb is clear of components (diagram 2) hence providing the best chance of providing the isolation required.

13. Ethernet ID Chip

All Acorn computer platforms have a chip built in as standard that contains a unique number. The intention of this is to provide a method of software protection. Acorn is now in the process of making a change to the ID contained in these IC's. An Ethernet number will be given to each machine produced. 24 bits of this number will be read from the ID chip and this then added to Acorn's base Ethernet number to provide the unique number required.

Acorn platform Ethernet ID's are calculated by the following :-

Read the DS2401 device to get a unique 24 bit number (Hex. XX XX XX).

Add this device number to the Acorn Base Ethernet Number of Hex. 00 00 A4 10 00 00.

This gives the value of the platform Ethernet number.

14. EMC

When designing for compliance the following points should be borne in mind.

- all external connectors should be a robust, recognised EMC design.
- all external connectors should have a comprehensive low impedance bond to the rear panel.
- the rear panel must be conductive and fitted to the host computer frame via low impedance fixings.
- when fitted, there should not be any continuous slot longer than 20mm
- any external cables must have an EMC performance that does not compromise the host computer system
- if external cables are required for the card, but not supplied, full details of the recommended cable, connectors and construction methods of the leads should be supplied
- a four layer PCB is preferred together with a good layout
- connection of the card volts line to the rear panel is not generally recommended, however , on some PCB designs this may be found to give an improvement in static immunity
- be aware that the rear panel may be subject to high current earth continuity testing
- the EMC performance of the card must not deteriorate as a result of insertion and removal during the life of the product

15. Safety

The current industry wide IT safety standard is IEC950 whose European 'harmonized' version is EN60950 / BS7002 but your particular application may also be within the scope of other additional standards. The main requirements are that the equipment provide protection against:

- the spread of fire
- hazardous voltages or energy

15.1 The spread of fire

The underwriters Laboratory (UL) of the USA have devised several standard ways of testing plastic materials for their flammability properties. The UL94 test procedure is used within IEC950 to specify the required flame retardant level for materials and components. The ratings start at 94v-0 down to 94v-1, 94v-2 and finally 94HB.

Confirmation of a UL test pass will be the issue of a 'yellow card', a copy of which can be obtained from your supplier, for either the plastic material itself or indeed the component.

IEC950 specifies that PCBs will have a minimum flame-retardancy rating of UL94v-1 and that any component is mounted on the PCB meets the lower standard of UL94v-2.

The choice and layout of components should also seek to prevent the spread of fire across the PCB and within the computer.

The computer external enclosure forms a fire barrier and as such its material must meet the higher standard of UL94v-1. As the network card rear panel will be part of the fire enclosure the panel itself must meet this standard; metal is acceptable.

If you fit a large plastic connector into this rear panel the connector will also have to be UL94v-1.

15.2 Hazardous voltages or energy.

The computer PSU is designed to provide only SELV (safety extra low voltage) to the computer. This means that the PCB supply voltages have two independent means of protection against hazardous voltages thus ensuring that even under single fault conditions the voltage on the computer PCB and interfaces will be safe. Within IEC950 hazardous voltages are those greater than 42.4 volts peak or 60 volts DC.

Physical access by a user to any hazardous voltages must be prevented by a physical barrier in which no aperture is greater than 5 mm in dimension.

Network Cards MUST be designed in such a way that they do not introduce either a reduction in fire protection or of voltage isolation into the host computer. Designers should obtain a copy of the standard and if necessary seek further clarification by consulting a reputable test facility such as BSI.

With the EEC Directive on General Product Liability manufacturers and importers within the Community are subject to strict liability. This existing law removes the plaintiff's requirements to prove that a product was 'defective' when seeking damages. The possession of an EN certification may not be an adequate defence and therefore manufacturers need to be aware that there may be safety aspects of their product which are not covered by the standards.

15.3 Testing.

U.K. legislation now requires that portable electrical equipment be tested regularly for safety reasons. Be aware that this testing may be carried out by a variety of people of varying technical competence and experience.

Class 1, earthed equipment will be tested by the application of a high current, low voltage, source of 4 - 25 Amps, between any exposed metalwork and the earth pin in the mains plug. the presence of your network card in the computer will make it liable for testing.

You should therefore consider whether to provide information in your documentation to either the user or the dealer on how your card should be tested.

15.4 Interworking with other 3rd party network cards.

Care should be taken that the network card is in compliance with relevant networking specifications. This should include testing to ensure that the developed card works successfully (and without losing packets) on a network comprising of a mix of manufacturers cards.

16. Installing

Access to the computer is straight forward and it is possible for users to perform this upgrade. The Welcome Guide, which is supplied with each system, includes information on how to enter the case. Instructions should therefore be given on how to fit the upgrade card and label and also how to test that it has been installed correctly.

17. Environmental Criteria

The Network Card must capable of meeting the following environmental conditions, whilst at no time requiring the host machine to exceed its own product specification:

17.1 Operating

The Network Card must continue to operate to specification and suffer neither mechanical nor electrical damage during and after the following applied environmental envelopes:

- Card environmental temperature:
  10 to 45 °C up to 1000 metres above sea level, reduced linearly down to
  25 °C at 2,500 metres.
- Thermal gradient:
  20 °C per hour, within the above limits.

- Humidity:
  20% to 80% RH at 45 °C, non-condensing.
- Altitude:
  -200 to 2,500 metres above sea level, subject to temperature reduction.
- Vibration:
  Random Vibration to BS 2011 Pt 2.1 Test fed with the following parameters:
  0 - 55 Hz 0.0004 g^2/Hz
  For a total of 1 hour.

17.2 Non-operating

As operating, except that the Network Card must suffer no adverse effects (including mechanical or electrical damage) after the following tests:

- Temperature
  4 to 50 °C
- Thermal shock:
  Between -20 and 50 °C temperature limits, 4 hours soak at each temperature, with a maximum transfer time of 5 minutes. Repeated 3 times to Acorn procedure 0980,530.
- Humidity:
  8 to 90% RH at 35 °C non-condensing.
- Altitude:
  -200 to 10,000 metres above sea level.
- Mechanical shock:
  3 parallel falls from a height of 50 mm.
- Vibration:
  Random vibration to BS 2011 Pt 2.1 test, fed with the following parameters:
  20 - 500 Hz 500 - 2000Hz
  0.02 g^2/Hz 0.02 g^2/Hz linearly decreasing to 0.001 g^2/Hz
  For a total of 6 hours; 2 hours in each perpendicular axis.

17.3 Shipment and storage

As non-operating, except that when packaged the unit must operate to specification and suffer neither mechanical nor electrical damage after the following tests. The packaging must still look undamaged after any of the following tests:

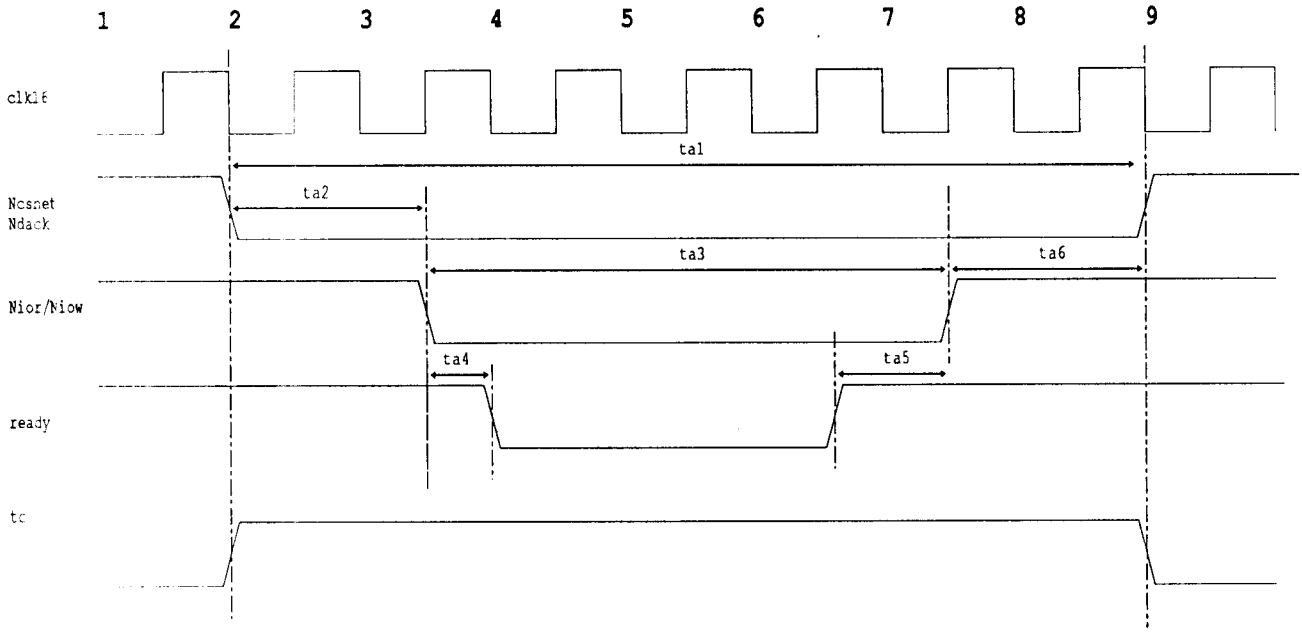
- Mechanical shock:
  Capable of withstanding one drop from 0.6 metres on any face, corner or edge.
- Sensitivity to electrostatic discharge:
  0 to 7.5kV; operation unimpaired
  7.5kV to 15kV: errors may occur but no permanent damage

18. Related Documents

Technical Reference Manual.
Programmer's Reference Manual.

Appendix A Timings for Product Variant A.

Programming for a type A I/O cycle.



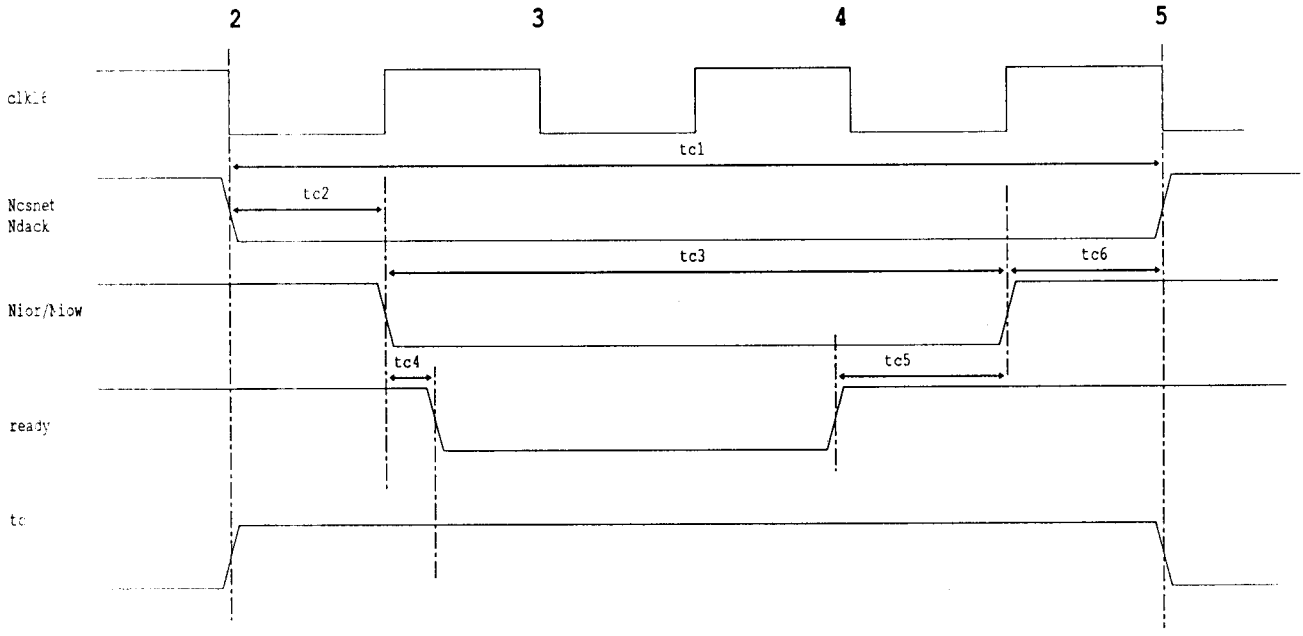
Sym.	Description	Min.	Typ.	Max.	Units	notes
ta1	Ncsnet strobe width		437		nS	
ta2	Ncsnet or dack low to Nior or Niow low		94		nS	
ta3	Nior and Niow strobe width		250		nS	(i)
ta4	Nior or Niow low to ready low		180		nS	(ii)
ta5	ready high to Nior or Niow high		125		nS	(ii)
ta6	Nior or Niow high to Ncsnet high		93		nS	

notes.

(i) The ready signal is used to stretch the present cycle if required. The maximum timings given are for non-stretched cycles.

(ii) There are two important timings associated with the stretched cycle. If the ready signal is not asserted early enough in the cycle this signal will not be seen and therefore the cycle will continue to complete without being stretched. When the stretched cycle is ready to be completed there is a variable delay between deasserting the ready signal and this being synchronised to the main system for completing.

Programming for a type C I/O cycle.



Sym.	Description	Min.	Typ.	Max.	Units	notes
tc1	Ncsnet strobe width		188		nS	
tc2	Ncsnet or dack low to Nior or Niow low		31		nS	
tc3	Nior and Niow strobe width		125		nS	(i)
tc4	Nior or Niow low to ready low	30			nS	(ii)
tc5	ready high to Nior or Niow high			125	nS	(ii)
tc6	Nior or Niow high to Ncsnet high		31		nS	

Notes.

(i) The ready signal is used to stretch the present cycle if required. The maximum timings given are for non-stretched cycles.

(ii) There are two important timings associated with the stretched cycle. If the ready signal is not asserted early enough in the cycle this signal will not be seen and therefore the cycle will continue to complete without being stretched. When the stretched cycle is ready to be completed there is a variable delay between deasserting the ready signal and this being synchronised to the main system for completing.

Appendix B Product specific (Psp) pin definitions

Product variant A - IOMD based system (such as Risc PC).

Psp8 assigned as Ndack0	DMA acknowledge input	TTL level
Psp7 assigned as Dreq0	DMA request output	TTL level
Psp6 assigned as Tc	Terminal Count	TTL level
Psp5 reserved		
Psp4 reserved		
Psp[3:1] are not connected		

Product variant B - Morris based system.

Psp[8:5] are not connected		
Psp4 assigned as AnlgBY	Analogue output channel B(Y)	Analogue level
Psp3 assigned as AnlgBX	Analogue output channel B(X)	Analogue level
Psp2 assigned as AnlgAY	Analogue output channel A(Y)	Analogue level
Psp1 assigned as AnlgAX	Analogue output channel A(X)	Analogue level